UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,034	09/12/2003	Paul J. Mantey	200309970-1	9298

22879 7590 07/25/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,034	MANTEY ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16-18,20,21,28-30,33,34,38 and 40-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16-18,20,21,28-30,33,34,38 and 40-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 14, 16 – 18, 20 – 21, 28 – 30, 33 – 34, 38, and 40 – 44 have been examined.

Claim Objections

Claim 17 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 17 recites essentially the same limitation as step (D) of claim 16.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 12 and 42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 12 and 42 recite "a second FIFO buffer coupled to the receive machine and coupled between the host processor and the

bus controller but not between the receive machine and the bus controller..." Examiner notes that as shown in Figure 2A of the Applicant's disclosure, a second FIFO buffer (226) is coupled between the receive machine (222) and the bus controller (208) via busses 230 and 228.

For purposes of examination, Examiner will assume that this limitation of claims 12 and 42 will be amended similarly to the amendment of the "... first first-in first-out (FIFO buffer)..." limitation.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 33 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Trang (U.S. 5,630,054).

Regarding claim 33, Trang describes a computer-implemented method comprising steps of:

(A) Initializing a receive checksum (column 5, lines 52 – 53);

(B) Receiving a first portion of a message over a communications bus (Figure 1, item 124; column 5, line 67 – column 6, line 2);

(C) Updating the receive checksum based on the first portion of the message (where the receive checksum is interpreted as a partial checksum value; column 6, lines 11 – 16);

(D) Receiving a subsequent portion of the message over the communications bus (column 6, lines 44 – 48);

(E) Updating the receive checksum based on the subsequent portion of the message (column 6, lines 54 – 60);

(F) After steps (A) – (E), transmitting the first and subsequent portions of the message to a host processor (Examiner notes that column 6, line 52 – column 7, line 16 provides a detailed description of the above claimed invention in the case of writing. In the case of reading from a disk to a host processor (interpreted as a host computer (110)), the same procedure is carried out, as described in column 7, line 64 – column 87, line 40);

Wherein steps (A) – (E) are performed without interrupting the host processor (Examiner interprets the processor as not being interrupted since Trang does not describe doing so.).

Regarding claim 34, Trang describes the method further comprising a step of:

(G) Repeating steps (D) – (E) until reception of the message is complete (column 7, lines 3 – 16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (U.S. 6,182,180) in view of Elliot (U.S. Pub. 2005/0055489).

Regarding claim 1, Liu et al. describe a computer system comprising:

A communications bus implemented in accordance with an Inter-IC bus specification (Figure 1, 2, item 107);

A bus controller coupled to the communications bus (where a bus controller may be interpreted as a system interface processor; column 6, lines 19 - 23);

A send machine (Figure 2, items 207) coupled between a host processor (Figure 1, item 101) and the bus controller (where a send machine may be interpreted as a message data register (MDR); column 7, lines 16 – 25);

A first first-in first-out (FIFO) buffer coupled to the send machine (where a FIFO buffer may be interpreted as a request queue; Figure 2, item 203).

Liu et al. fail to teach the first FIFO further coupled between the host processor and the bus controller over an internal bus, the first FIFO not being coupled to the send machine over the internal bus.

Elliot teaches a FIFO (Figure 2, item 60) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over an internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled i-data, i-add, t-data and t-add), the first FIFO not being coupled to the send machine (Figure 2, item 68) over the internal bus (Figure 2 shows the send machine coupled to the FIFO over the bus labeled fifo-ctrl) for the purpose of allowing different parts of the system to run at different clock rates, thereby improving bus efficiency (paragraphs 4, 7, 9).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the bus system of Elliot in the computer system of Liu et al. for the purpose of allowing different parts of the system to operate at different clock rates. This would have been obvious in order to improve bus efficiency.

Regarding claim 2, Liu et al. teach the computer system of claim 1, wherein the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor without interrupting the host processor (column 7, lines 25 – 26; Figure 2, items 203, 205 show that both queues are a size of 1K – either bits or bytes would meet the limitation of a plurality of bytes; column 10, lines 24 – 34 tell of how a messages is

placed into the request buffer, but note that the interrupt is not generated until a response is received from the I2C device).

Regarding claim 3, Liu et al. teach the computer system of claim 1, wherein:

The first FIFO buffer comprises means for receiving a plurality of bytes from the host processor ((column 7, lines 25 – 26; Figure 2, items 203, 205 show that both queues are a size of 1K – either bits or bytes would meet the limitation of a plurality of bytes);

The send machine comprises means for transmitting the plurality of bytes over the communications bus without interrupt the host processor (column 10, lines 24 – 34 tell of how a messages is placed into the request buffer and processed by the interface, but note that the interrupt is not generated until a response is received from the I2C device).

With regard to claim 4, Elliot teaches the additional limitation further comprising:

A receive machine coupled between the host processor and the bus controller (Figure 2, item 70);

A second FIFO buffer (Figure 2, item 62) coupled to the receive machine and coupled between the host processor and the bus controller.

* * *

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. in view of Elliot and Yoshida (U.S. 5,928,372).

Liu et al. and Elliot fail to teach wherein the receive machine comprises checksum generation means for generating a message checksum for a message while the message is being received by the bus controller over the communications bus.

Yoshida teaches a checksum generation means for generating a message checksum for a message while the message is being received by the bus controller over the communications bus (where checksum generation means may be interpreted as data check code generation circuits; column 11, lines 14 – 24).

It would have been obvious to one or ordinary skill in this art at the time of invention by applicant to combine the checksum generation means of Yoshida with the system of Liu et al. in order to provide for a means of verifying the data transmitted across the communications bus. This would have been obvious since error-free data is critical to the correct operation of a digital system.

* * *

Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. in view of Elliot and Feeney et al. (U.S. 6,072,781).

With regard to claim 6, Liu et al. describe the computer system of claim 1, further comprising:

Means for receiving a message from the host processor (Figure 2, items 203, 207; Figure 4A, item 420);

Means for attempting to send the message over the communications bus to a target device (Figure 4A, item 422);

Liu et al. and Elliot fail to teach:

Means for determining whether the message was received without errors by the target device;

Retry means for attempting again to send the message over the communication bus to the target device if it is determined that the message was not received without errors by the target;

Feeney et al. teach means for determining whether the message was received without errors through the use of FIFO status registers (Figures 13, 14; column 18, line 4 – column 20, line 12), and retry means for attempting again to send the message over the communication bus to the target if it is determined that the message was not received without errors by the target (column 16, lines 36 – 49 describe retrying messages that failed to send).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the means of retrying failed messages as taught by Feeney et al. into the computer system of Liu et al. and Elliot for the purpose of ensuring the delivery of messages on the communication bus.

With regard to claim 7, Feeney et al. teach the additional limitation wherein the retry means comprises means for attempting again to send the message over the communications bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device (column 16, lines 36 – 49 describe retrying a message without involving the processor).

With regard to claim 8, Feeney et al. teach the additional limitation wherein the retry means comprises means for attempting again to send the message over the communications bus to the target device without obtaining the message again from the host processor if it is determined that the message was not received without errors by the target device (column 16, lines 36 – 49 describe storing the message in a FIFO in order to allow the processor to move onto other tasks).

* * *

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. in view of Elliot and Cao et al. (U.S. 5,230,044).

Liu et al. and Elliot fail to teach a busfree count means for storing a busfree count associated with the computer system, a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use, and a fair arbitration block coupled between the host processor and the bus controller, the fair

arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use (where a busfree timer may be interpreted as a "quiet slot" counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by Cao et al. into the system of Liu et al. and Elliot for the purpose of providing arbitration amongst devices on the communications bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

* * *

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. and Elliot in view of Webb et al. (U.S.4,577,060).

With regard to claim 10, Liu et al. and Elliot fail to teach a byte timer coupled between the bus controller and the host processor.

Webb et al. teach a byte timer (where a byte timer may be interpreted as a no-response timer; column 13, lines 49 - 60).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the byte timer as taught by Webb et al. into the system of Liu et al. and Elliot. This would have been obvious in order to provide a method of ensuring that a communication link (or bus) is operating properly, and prevent the system from wasting time sending messages to processors/terminals that are not responsive (column 14, lines 11 – 19).

With regard to claim 11, Webb et al. teach the additional limitation wherein the byte timer (interpreted as a no-response timer) comprises means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed (where a host processor may be interpreted as a terminal; where generating a signal indicating the processor has failed may be interpreted as marking a terminal as being "offline" or "down"; column 13, line 49 – column 14, line 30).

* * *

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (U.S. 6,122,758) in view of Elliot.

Regarding claim 12, Johnson et al. teach a computer system comprising:

A communications bus implemented in accordance with an Inter-IC bus specification (Figure 4, 7, item 310; column 7, lines 10 - 12);

A bus controller coupled to the communications bus (where a bus controller may be interpreted as a system interface processor; column 11, lines 31 – 36, 61 - 65);

A send machine (Figure 7, item 707) coupled between a host processor (Figure 4, item 200) and the bus controller (where a send machine may be interpreted as a message data register (MDR); column 12, lines 17 – 32), the send machine comprising means for transmitting the plurality of bytes over the communications bus without interrupting the host processor (column 14, lines 18 – 38, and column 15, lines 40 - 51 tell of how a messages is placed into the request buffer and processed by the interface, but note that the interrupt may not be generated until a response is received from the I2C device).

A first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller (where a FIFO buffer may be interpreted as a request queue; Figure 7, item 516; column 12, lines 7 - 10, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor (column 12, lines 26 - 30; Figure 7, items 516, 514 show

that both queues are a size of 1K – either bits or bytes would meet the limitation of a plurality of bytes; column 15, lines 40 – 51 tell of how a messages is placed into the request buffer, but note that the interrupt is not generated until a response is received from the I2C device).

A receive machine (Figure 7, item 707) coupled between the host processor and the bus controller (where a receive machine may be interpreted as a message data register (MDR); column 12, lines 17 – 32), the receive machine comprising means for receiving the plurality of bytes over the communications bus without interrupting the host processor (column 14, lines 18 – 38; column 15, lines 40 – 51 tell of how the response bytes are written into the response FIFO, and the if directed to do so by the device driver, an interrupt is asserted. Examiner interprets this to mean that the device driver may also *not* be directed to assert an interrupt, and therefore the reference teaches the limitation of receiving the plurality of bytes without interrupting the processor).

A second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller (where a FIFO buffer may be interpreted as a response queue; Figure 7, item 514; column 12, lines 10 –14), the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (column 14, lines 18 – 38; column 15, lines 40 – 51 tell of how the response bytes are written into the response FIFO, and the if directed to do so by the device driver, an interrupt is asserted. Examiner interprets this to mean that the device driver may also *not* be directed to assert an interrupt, and therefore the

reference teaches the limitation of receiving the plurality of bytes without interrupting the processor).

Johnson et al. fail to teach the first FIFO coupled between the host processor and the bus controller over an internal bus, the first FIFO not being coupled to the send machine over the internal bus. Additionally, Johnson et al. fail to teach the second FIFO coupled between the host processor and the bus controller over an internal bus, the second FIFO not being coupled to the receive machine over the internal bus.

Elliot teaches a first FIFO (Figure 2, item 60) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over an internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled i-data, i-add, t-data and t-add), the first FIFO not being coupled to the send machine (Figure 2, item 68) over the internal bus (Figure 2 shows the send machine coupled to the FIFO over the bus labeled fifo-ctrl). Elliot also teaches a second FIFO (Figure 2, item 62) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over an internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled I-r-data, t-r-data), the second FIFO not being coupled to the receive machine (Figure 2, item 70) over the internal bus (Figure 2 shows the receive machine coupled to the FIFO over the bus labeled fifo-ctrl) for the purpose of allowing different parts of the system to run at different clock rates, thereby improving bus efficiency (paragraphs 4, 7, 9).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the bus system of Elliot in the computer

system of Johnson et al. for the purpose of allowing different parts of the system to operate at different clock rates. This would have been obvious in order to improve bus efficiency.

* * *

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Elliot, Feeney et al., Cao et al., and further in view of Webb et al.

Johnson et al. teach a computer system of claim 12 further comprising:

Means for receiving a message from the host processor (Figure 7, items 516, 707; column 12, lines 26 – 32);

Means for attempting to send the message over the communications bus to a target device (column 15, lines 15 – 36 give an example of how a message is sent over the communications bus to a target device (microcontroller)).

Means for determining whether the message was received without errors by the target device (column 15, lines 62 – 64).

Johnson et al. fail to describe a retry means, a busfree count means, a busfree count timer, a fair arbitration block, and a byte timer.

Feeney et al. teach retry means for attempting again to send the message over the communications bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device

(column 16, lines 36 – 49 describe retrying messages that failed to send; column 16, lines 36 – 49 describe retrying a message without involving the processor).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the means of retrying failed messages as taught by Feeney et al. into the computer system of Liu et al for the purpose of ensuring the delivery of messages on the communication bus.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use (where a busfree timer may be interpreted as a "quiet slot" counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by Cao et al. into the system of Johnson et al., Elliot, and Feeney et al, for the purpose of providing arbitration amongst devices on the communications bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use

of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

Webb et al. teach a byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed (where a byte timer may be interpreted as a no-response timer; column 13, lines 49 – 60; where a host processor may be interpreted as a terminal; where generating a signal indicating the processor has failed may be interpreted as marking a terminal as being "offline or "down"; column 13, line 49 – column 14, line 30).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the byte timer as taught by Webb et al. into the system of Johnson et al., Elliot, Feeney et al., and Cao et al. This would have been obvious in order to provide a method of ensuring that a communication link (or bus) is operating properly, and prevent the system from wasting time sending messages to processors/terminals that are not responsive (column 14, lines 11 – 19).

* * *

Claims 14, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Regis (EP 1 174 798 A2) in view of what is well known in the art as evidenced by Davidson et al. (U.S. 5,613,157) and Quicksall (U.S. 6,449,289).

Regarding claim 14, Regis teaches a method for transmitting a message comprising a plurality of bytes over a communications bus, the method comprising steps of:

(A) Receiving at least two of the plurality of bytes from a host processor (Figure 7, item 32; page 6, lines 31 – 32 teach that a message can be up to 512 bytes; page 6, lines 45 - 46);

(B) Transmitting the at least two of the plurality of bytes over the communications bus (Figure 7, item 28) without interrupting the host processor (paragraph 52)

(C) After step (B), interrupting the host processor (paragraph 65);

Regis fails to teach the communications bus in accordance with an Inter-IC bus.

Examiner takes Official Notice that it is well known in this art to use an Inter-IC bus for the purpose of connecting multiple processors to one another as evidenced by Davidson et al. (Figure 1, item 26) and Quicksall (Figure 2, item 11).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the Inter-IC bus as evidenced by Davidson et al. and Quicksall into the method of Regis for the purpose of providing a bus with a low pin count, and therefore, lower cost to manufacture.

Regarding claim 16, Andrews et al. teach the additional limitation comprising a step of:

(D) prior to step (B), storing the at least two of the plurality bytes in a buffer (interpreted as the transmit FIFO 24) without interrupting the host processor (paragraph 51);

wherein step (B) comprises steps of:

(B) (1) retrieving the at least two bytes from the buffer;

(B) (2) transmitting the at least two bytes over the bus without interrupting the host processor (paragraphs 52 – 53).

Regarding claim 17, Regis teaches the additional limitation wherein step (D) comprises a step of storing the plurality of bytes of the message in a buffer without interrupting the host processor (paragraphs 52 – 53).

* * *

Claims 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Regis in view of what is well known in the art as evidenced by Davidson et al. and Quicksall.

Regarding claim 18, Regis teaches a device for transmitting a message comprising a plurality of bytes over a communications bus, the device comprising:

Means for receiving at least two of the plurality of bytes from the host processor (Figure 7, item 32; page 6, lines 31 – 32 teach that a message can be up to 512 bytes; page 6, lines 45 - 46);

Means for transmitting the at least two of the plurality of bytes over the communications bus (Figure 7, item 28) without interrupting the host processor (paragraph 52);

Means for interrupting the host processor after the means for receiving receives the at least two of the plurality of bytes from the host processor (paragraph 65);

Regis fails to teach the communications bus in accordance with an Inter-IC bus.

Examiner takes Official Notice that it is well known in this art to use an Inter-IC bus for the purpose of connecting multiple processors to one another as evidenced by Davidson et al. (Figure 1, item 26) and Quicksall (Figure 2, item 11).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the Inter-IC bus as evidenced by Davidson et al. and Quicksall into the method of Regis for the purpose of providing a bus with a low pin count, and therefore, lower cost to manufacture.

Regarding claim 20, Regis teaches the additional limitation comprising:

Means for storing the at least two of the plurality of bytes in a buffer (interpreted as the transmit FIFO 24) without interrupting the host processor before the means for transmitting transmits the at least two of the plurality of bytes over the communications bus (Figure 7, item 28; paragraph 52);

Wherein the means for transmitting comprises:

Means for retrieving the at least two bytes from the buffer;

Means for transmitting the at least two bytes of the message over the bus without interrupting the host processor (paragraphs 52 – 53).

Regarding claim 21, Regis teaches the additional limitation wherein the means for storing comprises means for storing the plurality of bytes of the message in a buffer without interrupting the host processor (paragraphs 52 – 53).

* * *

Claims 28 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Regis in view of what is well known in the art as evidenced by Davidson et al. and Quicksall.

Regarding claim 28, Regis teaches a method for transmitting a message comprising a plurality of bytes from a source device having a first host processor to a destination device having a second host processor over a communications bus, the method comprising steps of:

(A) At the source device (Figure 7, item 34), receiving at least two of the plurality of bytes from the first host processor (Figure 7, item 32; page 6, lines 31 – 32 teach that a message can be up to 512 bytes; page 6, lines 45 - 46);

(B) At the source device, storing the at least two of the plurality of bytes in a first buffer (Figure 7, item 24; paragraph 51);

(C) At the source device, transmitting the at least two bytes of the message from the first buffer to the destination device (Figure 7, item 134) over the communications bus (Figure 7, item 28) without interrupting the first host processor (paragraph 52);

(D) At the destination device, receiving the at least two bytes of the message without interrupting the second host processor (paragraphs 52, 53);

(E) At the destination device, storing the at least two bytes in a second buffer (Figure 7, item 126);

(F) At the destination device, transmitting the at least two bytes from the second buffer to the second host processor (paragraphs 53, 54).

Regis fails to teach the communications bus in accordance with an Inter-IC bus.

Examiner takes Official Notice that it is well known in this art to use an Inter-IC bus for the purpose of connecting multiple processors to one another as evidenced by Davidson et al. (Figure 1, item 26) and Quicksall (Figure 2, item 11).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the Inter-IC bus as evidenced by Davidson et al. and Quicksall into the method of Regis for the purpose of providing a bus with a low pin count, and therefore, lower cost to manufacture.

Regarding claim 29, Regis teaches the additional limitation wherein the step (B) comprises a step of storing the at least two of the plurality of bytes in the first buffer without interrupting the first host processor (Examiner notes that Regis does not say it interrupts the processor at this point, and so it is interpreted to not; paragraphs 51, 52).

Regarding claim 30, Regis teaches the additional limitation wherein the step (E) comprises a step of storing the at least two of the plurality of bytes in the second buffer without interrupting the second host processor (Examiner notes that Regis does not say it interrupts the processor at this point, and so it is interpreted to not; paragraphs 52, 54).

* * *

Claims 38, 40, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. in view of Cao et al. and Hughes et al. (U.S. 6,266,744).

Liu et al. teach a communications bus in accordance with an Inter-IC bus specification and a bus controller coupled to the communications bus (Figure 1, 2, item 107; where a bus controller may be interpreted as a system interface processor; column 6, lines 19 – 23) but fail to teach a busfree count means for storing a busfree count associated with the computer system, a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use, and a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use (where a busfree timer may be interpreted as a "quiet slot" counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by Cao et al. into the system of Liu et al. for the purpose of providing arbitration amongst devices on the communications bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

Liu et al. and Cao et al. both fail to teach the fair arbitration block modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal, the arbitration means comprising:

Priority means for generating the priority signal;

Modifier storage means for storing a plurality of busfree count modifiers;

Selection means for selecting one of the plurality of busfree count modifiers based on the priority signal;

Modification means for modifying the default busfree count based on the selected one of the plurality of busfree count modifiers to produce the arbitrated busfree count signal.

Hughes et al. teach modifying a busfree count (interpreted as "backoff time"; column 39, lines 59 – 62) according to a priority signal to produce an arbitrated busfree count signal, the arbitration means comprising:

Priority means (Figure 21, item 66) for generating the priority signal (interpreted as the signal entering item 334 from the right side);

Modifier storage means for storing a plurality of busfree count modifiers (Figure 21, item 330; column 40, lines 50 – 57);

Selection means for selecting of the plurality of busfree count modifiers based on the priority signal (Figure 21, item 334; column 40, line 66 – column 41, line 1);

Modification means for modifying the default busfree count based on the selected one of the plurality of busfree count modifiers to produce the arbitrated busfree count signal (column 39, lines 31 – 35).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count selection means as taught by Hughes et al. into the device of Liu et al. and Cao et al. for the purpose of selecting a variable amount of time for a device to wait before re-attempting arbitration.

This would have been obvious in order to make the arbitration process more equitable, thus improving system performance.

Regarding claim 40, Hughes et al. teach the additional limitation wherein the modifier storage means comprises a plurality of registers (Figure 21, item 330; column 40, lines 50 – 57).

Regarding claim 41, Hughes et al. teach the additional limitation wherein the selection means comprises a multiplexer (Figure 21, item 334; column 40, line 66 – column 41, line 1).

* * *

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Elliot, Feeney et al., Cao et al., and Webb et al.

Regarding claim 42, Johnson et al. teach a computer system comprising:

A communications bus implemented in accordance with an Inter-IC bus specification (Figure 4, 7, item 310; column 7, lines 10 - 12);

A bus controller coupled to the communications bus (where a bus controller may be interpreted as a system interface processor; column 11, lines 31 – 36, 61 - 65);

A send machine (Figure 7, item 707) coupled between a host processor (Figure 4, item 200) and the bus controller (where a send machine may be interpreted as a

message data register (MDR); column 12, lines 17 – 32), the send machine comprising means for transmitting the plurality of bytes over the communications bus without interrupting the host processor (column 14, lines 18 – 38, and column 15, lines 40 - 51 tell of how a messages is placed into the request buffer and processed by the interface, but note that the interrupt may not be generated until a response is received from the I2C device).

A first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller (where a FIFO buffer may be interpreted as a request queue; Figure 7, item 516; column 12, lines 7 - 10, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor (column 12, lines 26 - 30; Figure 7, items 516, 514 show that both queues are a size of 1K – either bits or bytes would meet the limitation of a plurality of bytes; column 15, lines 40 – 51 tell of how a messages is placed into the request buffer, but note that the interrupt is not generated until a response is received from the I2C device).

A receive machine (Figure 7, item 707) coupled between the host processor and the bus controller (where a receive machine may be interpreted as a message data register (MDR); column 12, lines 17 – 32), the receive machine comprising means for receiving the plurality of bytes over the communications bus without interrupting the host processor (column 14, lines 18 – 38; column 15, lines 40 – 51 tell of how the response bytes are written into the response FIFO, and the if directed to do so by the device driver, an interrupt is asserted. Examiner interprets this to mean that the device

driver may also *not* be directed to assert an interrupt, and therefore the reference teaches the limitation of receiving the plurality of bytes without interrupting the processor).

A second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller (where a FIFO buffer may be interpreted as a response queue; Figure 7, item 514; column 12, lines 10 –14), the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (column 14, lines 18 – 38; column 15, lines 40 – 51 tell of how the response bytes are written into the response FIFO, and the if directed to do so by the device driver, an interrupt is asserted. Examiner interprets this to mean that the device driver may also *not* be directed to assert an interrupt, and therefore the reference teaches the limitation of receiving the plurality of bytes without interrupting the processor).

Means for receiving a message from the host processor (Figure 7, items 516, 707; column 12, lines 26 – 32);

Means for attempting to send the message over the communications bus to a target device (column 15, lines 15 – 36 give an example of how a message is sent over the communications bus to a target device (microcontroller)).

Means for determining whether the message was received without errors by the target device (column 15, lines 62 – 64).

Johnson et al. fail to teach the first FIFO coupled between the host processor and the bus controller over an internal bus, the first FIFO not being coupled to the send

machine over the internal bus. Additionally, Johnson et al. fail to teach the second FIFO coupled between the host processor and the bus controller over an internal bus, the second FIFO not being coupled to the receive machine over the internal bus.

Elliot teaches a first FIFO (Figure 2, item 60) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over an internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled i-data, i-add, t-data and t-add), the first FIFO not being coupled to the send machine (Figure 2, item 68) over the internal bus (Figure 2 shows the send machine coupled to the FIFO over the bus labeled fifo-ctrl). Elliot also teaches a second FIFO (Figure 2, item 62) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over an internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled I-r-data, t-r-data), the second FIFO not being coupled to the receive machine (Figure 2, item 70) over the internal bus (Figure 2 shows the receive machine coupled to the FIFO over the bus labeled fifo-ctrl) for the purpose of allowing different parts of the system to run at different clock rates, thereby improving bus efficiency (paragraphs 4, 7, 9).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the bus system of Elliot in the computer system of Johnson et al. for the purpose of allowing different parts of the system to operate at different clock rates. This would have been obvious in order to improve bus efficiency.

Johnson et al. fail to describe a retry means, a busfree count means, a busfree count timer, a fair arbitration block, and a byte timer.

Feeney et al. teach retry means for attempting again to send the message over the communications bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device (column 16, lines 36 – 49 describe retrying messages that failed to send; column 16, lines 36 – 49 describe retrying a message without involving the processor).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the means of retrying failed messages as taught by Feeney et al. into the computer system of Johnson et al. for the purpose of ensuring the delivery of messages on the communication bus.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use (where a busfree timer may be interpreted as a "quiet slot" counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by Cao et al. into the system of Johnson et al. for the purpose of providing arbitration amongst devices on the communications bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

Webb et al. teach a byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed (where a byte timer may be interpreted as a no-response timer; column 13, lines 49 – 60; where a host processor may be interpreted as a terminal; where generating a signal indicating the processor has failed may be interpreted as marking a terminal as being "offline or "down"; column 13, line 49 – column 14, line 30).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the byte timer as taught by Webb et al. into the system of Johnson et al. This would have been obvious in order to provide a method of ensuring that a communication link (or bus) is operating properly, and prevent the system from wasting time sending messages to processors/terminals that are not responsive (column 14, lines 11 – 19).

* * *

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Elliot.

Regarding claim 43, Johnson et al. teach a computer system comprising:

A communications bus implemented in accordance with an Inter-IC bus specification (Figure 4, 7, item 310; column 7, lines 10 - 12);

A bus controller coupled to the communications bus (where a bus controller may be interpreted as a system interface processor; column 11, lines 31 – 36, 61 - 65);

A send machine (Figure 7, item 707) coupled between a host processor (Figure 4, item 200) and the bus controller (where a send machine may be interpreted as a message data register (MDR); column 12, lines 17 – 32), the send machine comprising means for transmitting the plurality of bytes over the communications bus without interrupting the host processor (column 14, lines 18 – 38, and column 15, lines 40 - 51 tell of how a messages is placed into the request buffer and processed by the interface, but note that the interrupt may not be generated until a response is received from the I2C device).

A first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller (where a FIFO buffer may be interpreted as a request queue; Figure 7, item 516; column 12, lines 7 - 10, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor (column 12, lines 26 - 30; Figure 7, items 516, 514 show that both queues are a size of 1K – either bits or bytes would meet the limitation of a plurality of bytes; column 15, lines 40 – 51 tell of how a messages is placed into the

request buffer, but note that the interrupt is not generated until a response is received from the I2C device).

A receive machine (Figure 7, item 707) coupled between the host processor and the bus controller (where a receive machine may be interpreted as a message data register (MDR); column 12, lines 17 – 32), the receive machine comprising means for receiving the plurality of bytes over the communications bus without interrupting the host processor (column 14, lines 18 – 38; column 15, lines 40 – 51 tell of how the response bytes are written into the response FIFO, and the if directed to do so by the device driver, an interrupt is asserted. Examiner interprets this to mean that the device driver may also *not* be directed to assert an interrupt, and therefore the reference teaches the limitation of receiving the plurality of bytes without interrupting the processor).

A second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller (where a FIFO buffer may be interpreted as a response queue; Figure 7, item 514; column 12, lines 10 –14), the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (column 14, lines 18 – 38; column 15, lines 40 – 51 tell of how the response bytes are written into the response FIFO, and the if directed to do so by the device driver, an interrupt is asserted. Examiner interprets this to mean that the device driver may also *not* be directed to assert an interrupt, and therefore the reference teaches the limitation of receiving the plurality of bytes without interrupting the processor).

Johnson et al. fail to teach the first FIFO coupled between the host processor and the bus controller over an internal bus, the first FIFO not being coupled to the send machine over the internal bus. Additionally, Johnson et al. fail to teach the second FIFO coupled between the host processor and the bus controller over an internal bus, the second FIFO not being coupled to the receive machine over the internal bus.

Elliot teaches a first FIFO (Figure 2, item 60) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over an internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled i-data, i-add, t-data and t-add), the first FIFO not being coupled to the send machine (Figure 2, item 68) over the internal bus (Figure 2 shows the send machine coupled to the FIFO over the bus labeled fifo-ctrl). Elliot also teaches a second FIFO (Figure 2, item 62) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over a second internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled I-r-data, t-r-data), the second FIFO not being coupled to the receive machine (Figure 2, item 70) over the internal bus (Figure 2 shows the receive machine coupled to the FIFO over the bus labeled fifo-ctrl) for the purpose of allowing different parts of the system to run at different clock rates, thereby improving bus efficiency (paragraphs 4, 7, 9).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the bus system of Elliot in the computer system of Johnson et al. for the purpose of allowing different parts of the system to

operate at different clock rates. This would have been obvious in order to improve bus efficiency.

* * *

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Elliot, and Cao et al.

Regarding claim 44, Johnson et al. teach a device for use in a computer system including a communications bus (Figure 4, 7, item 310; column 7, lines 10 - 12) and a bus controller coupled to the communications bus (where a bus controller may be interpreted as a system interface processor; column 11, lines 31 – 36, 61 - 65), the device comprising:

A send machine (Figure 7, item 707) coupled between a host processor (Figure 4, item 200) and the bus controller (where a send machine may be interpreted as a message data register (MDR); column 12, lines 17 – 32), the send machine comprising means for transmitting the plurality of bytes over the communications bus without interrupting the host processor (column 14, lines 18 – 38, and column 15, lines 40 - 51 tell of how a messages is placed into the request buffer and processed by the interface, but note that the interrupt may not be generated until a response is received from the I2C device).

A first first-in first-out (FIFO) buffer coupled to the send machine and coupled between the host processor and the bus controller (where a FIFO buffer may be

interpreted as a request queue; Figure 7, item 516; column 12, lines 7 - 10, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor (column 12, lines 26 - 30; Figure 7, items 516, 514 show that both queues are a size of 1K – either bits or bytes would meet the limitation of a plurality of bytes; column 15, lines 40 – 51 tell of how a messages is placed into the request buffer, but note that the interrupt is not generated until a response is received from the I2C device).

A receive machine (Figure 7, item 707) coupled between the host processor and the bus controller (where a receive machine may be interpreted as a message data register (MDR); column 12, lines 17 – 32), the receive machine comprising means for receiving the plurality of bytes over the communications bus without interrupting the host processor (column 14, lines 18 – 38; column 15, lines 40 – 51 tell of how the response bytes are written into the response FIFO, and the if directed to do so by the device driver, an interrupt is asserted. Examiner interprets this to mean that the device driver may also *not* be directed to assert an interrupt, and therefore the reference teaches the limitation of receiving the plurality of bytes without interrupting the processor).

A second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller (where a FIFO buffer may be interpreted as a response queue; Figure 7, item 514; column 12, lines 10 –14), the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (column 14, lines 18 – 38; column 15, lines 40 – 51 tell

of how the response bytes are written into the response FIFO, and the if directed to do so by the device driver, an interrupt is asserted. Examiner interprets this to mean that the device driver may also *not* be directed to assert an interrupt, and therefore the reference teaches the limitation of receiving the plurality of bytes without interrupting the processor).

Johnson et al. fail to teach the first FIFO coupled between the host processor and the bus controller over an internal bus, the first FIFO not being coupled to the send machine over the internal bus. Additionally, Johnson et al. fail to teach the second FIFO coupled between the host processor and the bus controller over an internal bus, the second FIFO not being coupled to the receive machine over the internal bus.

Elliot teaches a first FIFO (Figure 2, item 60) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over an internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled i-data, i-add, t-data and t-add), the first FIFO not being coupled to the send machine (Figure 2, item 68) over the internal bus (Figure 2 shows the send machine coupled to the FIFO over the bus labeled fifo-ctrl). Elliot also teaches a second FIFO (Figure 2, item 62) coupled between a host processor (Figure 1, item 12) and a bus controller (Figure 1, item 42; paragraph 23) over a second internal bus (interpreted as Figure 1, item 40 and the signals in Figure 2 labeled I-r-data, t-r-data), the second FIFO not being coupled to the receive machine (Figure 2, item 70) over the internal bus (Figure 2 shows the receive machine coupled to the FIFO over the bus labeled fifo-ctrl) for the purpose of

allowing different parts of the system to run at different clock rates, thereby improving bus efficiency (paragraphs 4, 7, 9).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the bus system of Elliot in the computer system of Johnson et al. for the purpose of allowing different parts of the system to operate at different clock rates. This would have been obvious in order to improve bus efficiency.

Johnson et al. fail to describe a busfree count means, a busfree timer, and a fair arbitration block.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications bus after the communications bus becomes available for use (where a busfree timer may be interpreted as a "quiet slot" counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by

Cao et al. into the system of Johnson et al. for the purpose of providing arbitration amongst devices on the communications bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MDS